

FIG. 1

ADAPTIVE COMPUTING ENGINE (ACE)

100

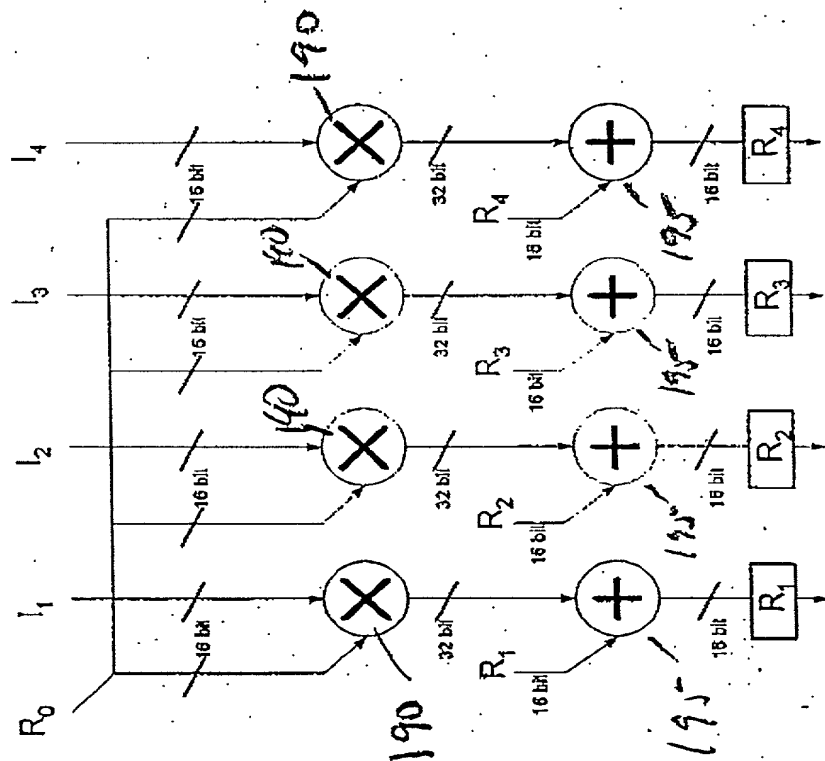


FIG. 2

TO OTHER MATRICES 150
(INCLUDING CONTROLLER 120 AND
MEMORY 140)

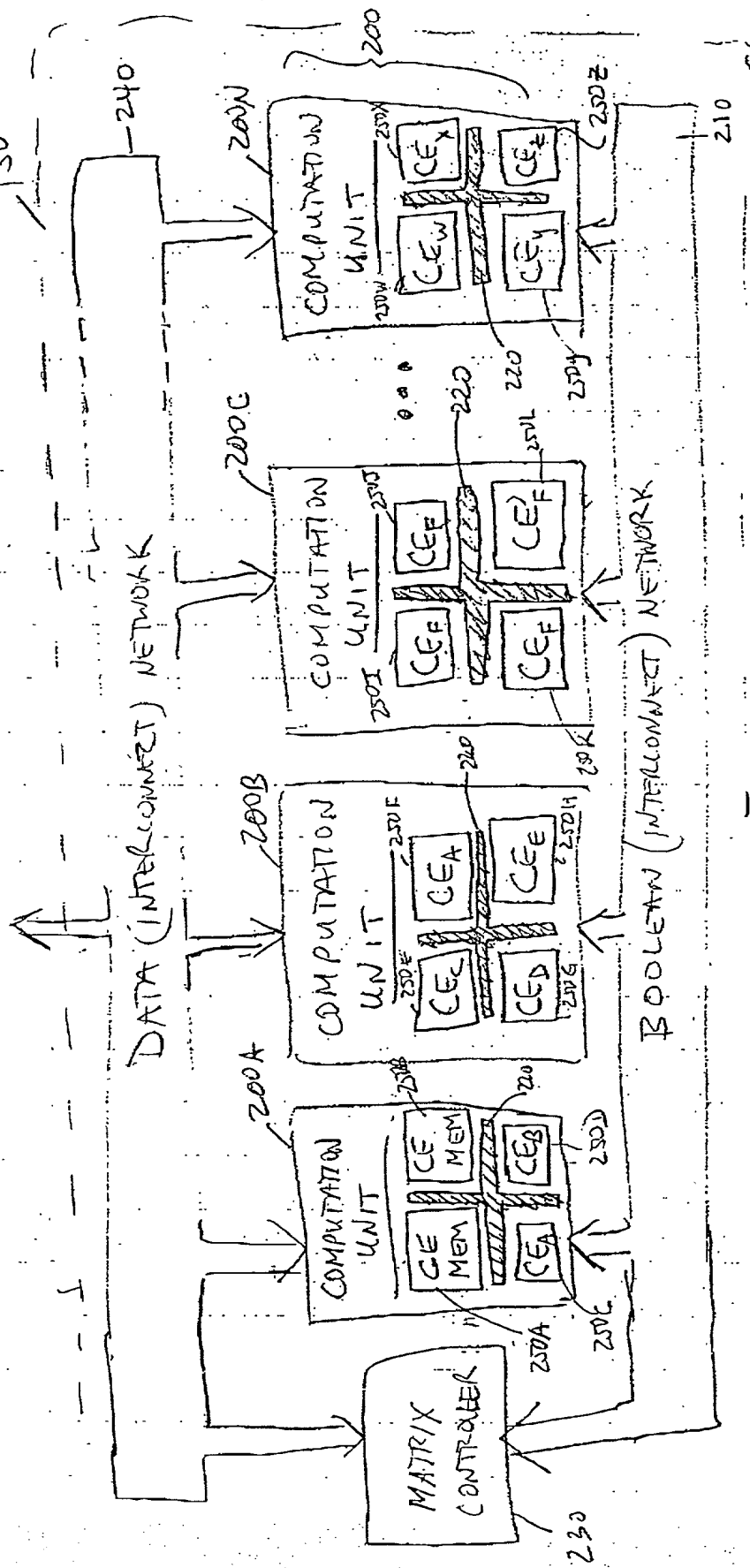


FIG. 3

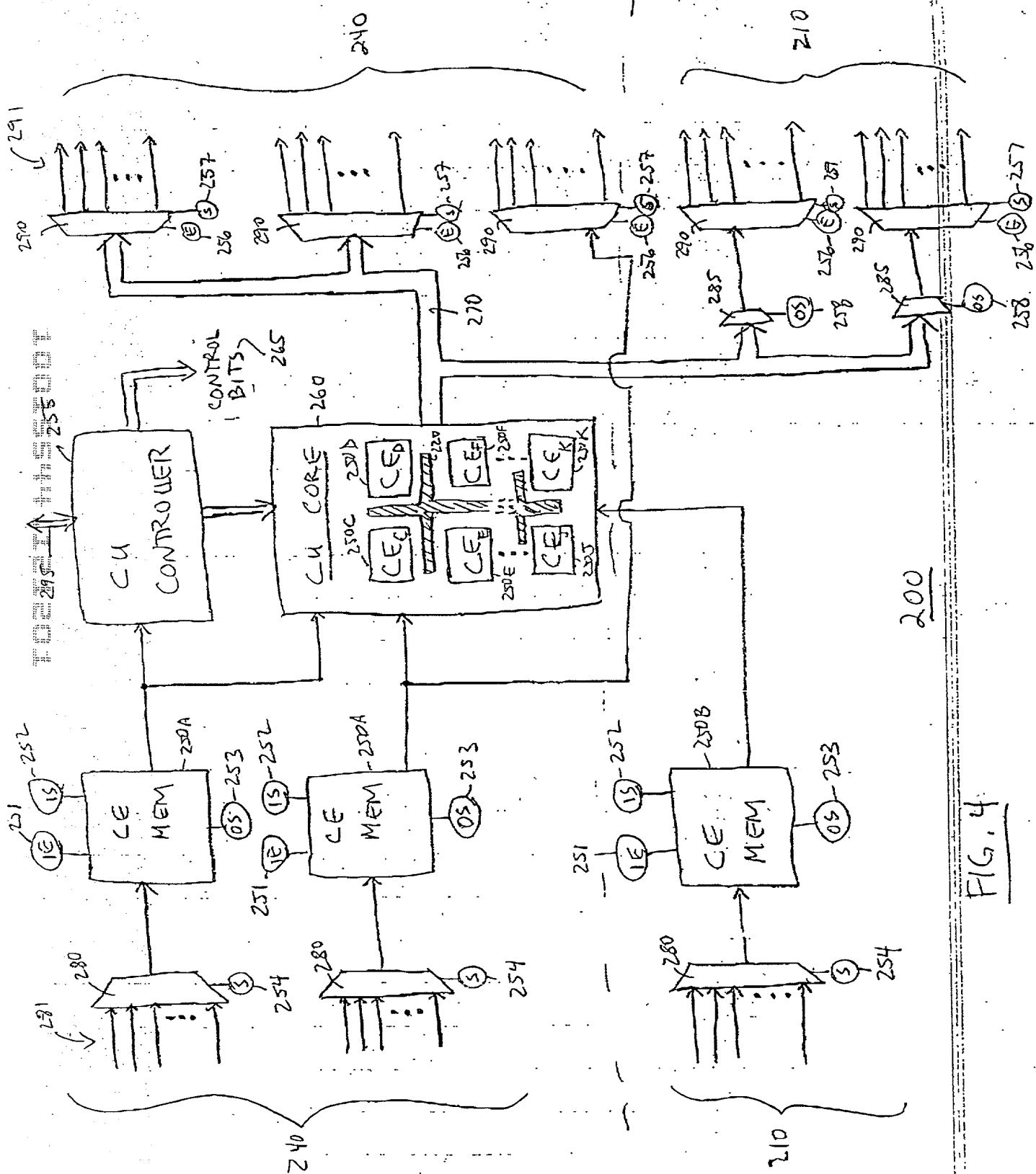


FIG. 4

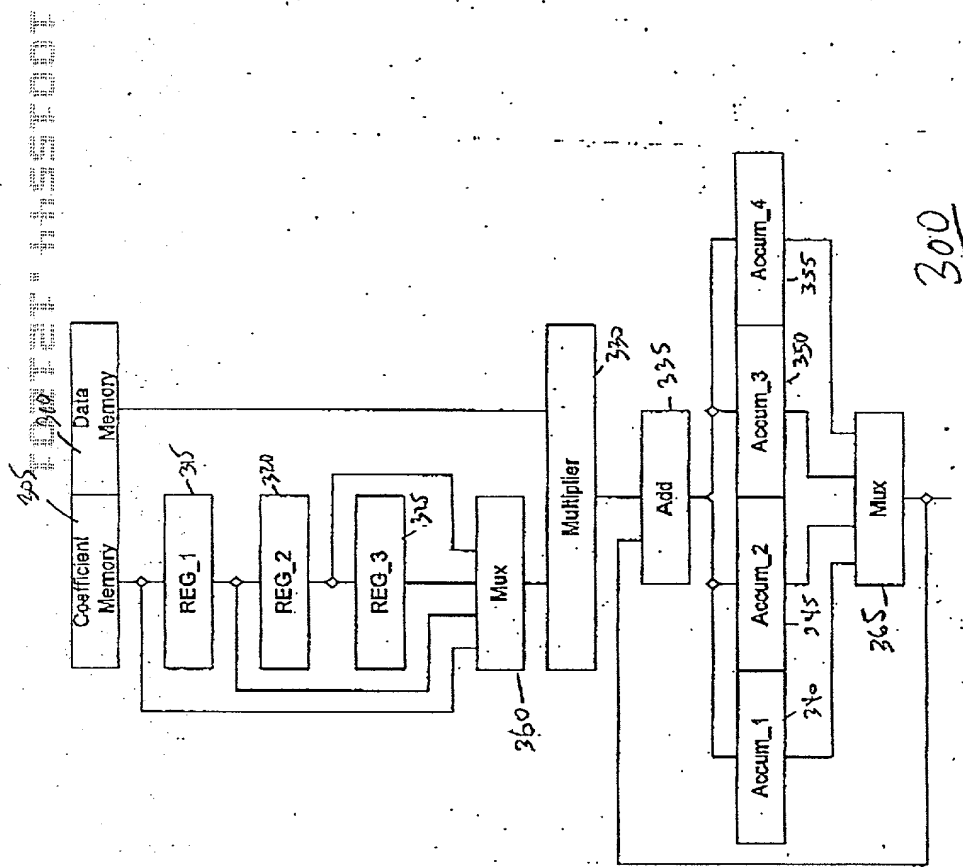


Fig. 5A

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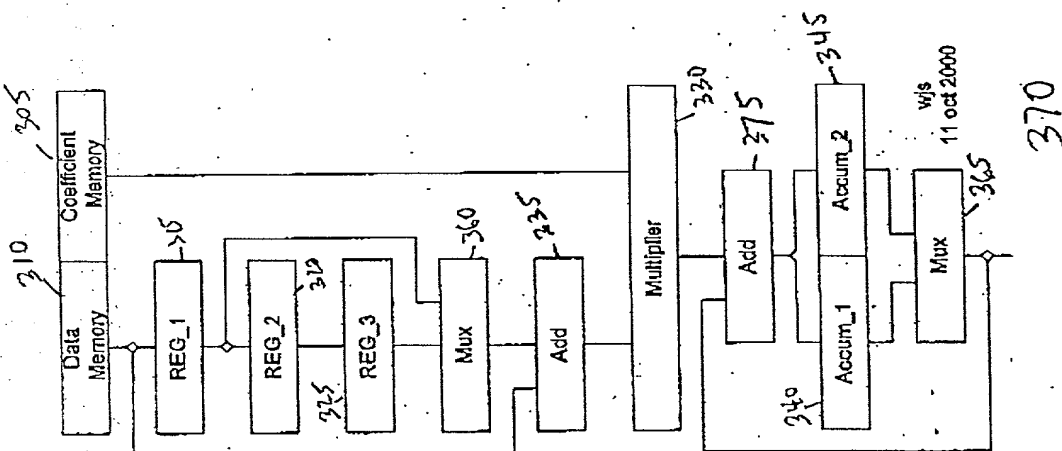


FIG. 5B

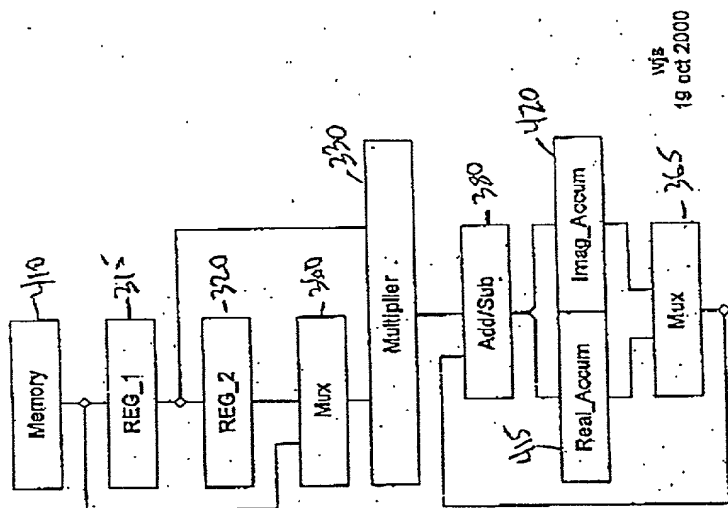
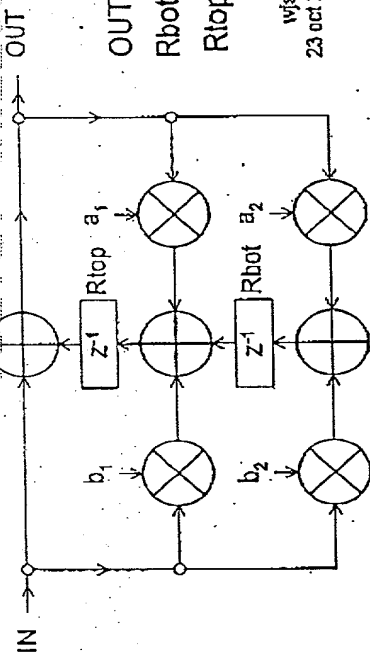


FIG. 5D

19 oct 2000

440

460



$$\begin{aligned} \text{OUT} &\leftarrow \text{IN} + \text{Rtop} \\ \text{Rbot} &\leftarrow \text{IN} * b_2 + \text{OUT} * a_2 \\ \text{Rtop} &\leftarrow \text{IN} * b_1 + \text{OUT} * a_1 + \text{Rbot} \end{aligned}$$

vjs
23 oct 2000

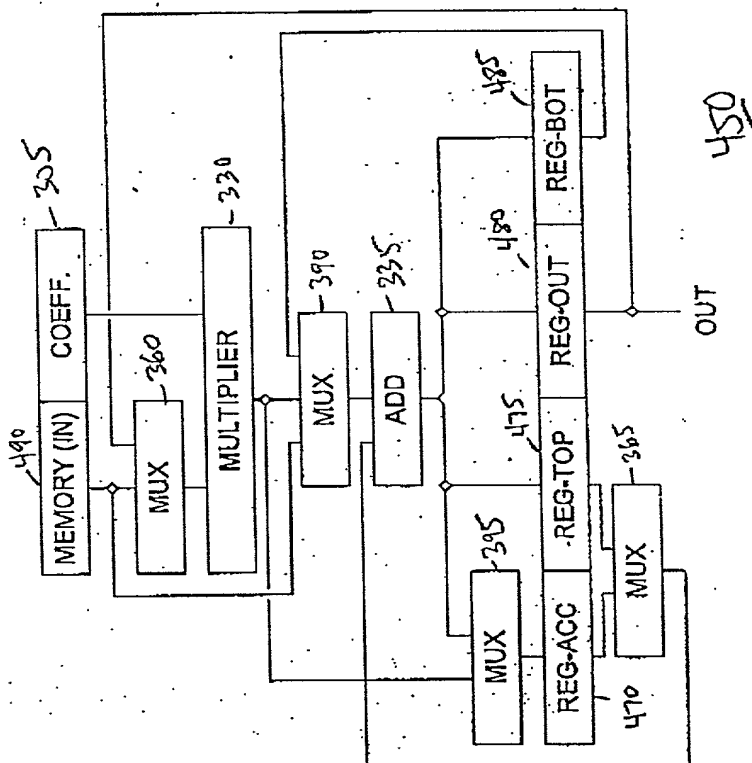


FIG. 5E

QUAD IN
PEER 3
PEER 2
PEER 1

505

REAL TIME INPUT

NODE INPUT
ARBITER GRANTS

510A

MUX

510B

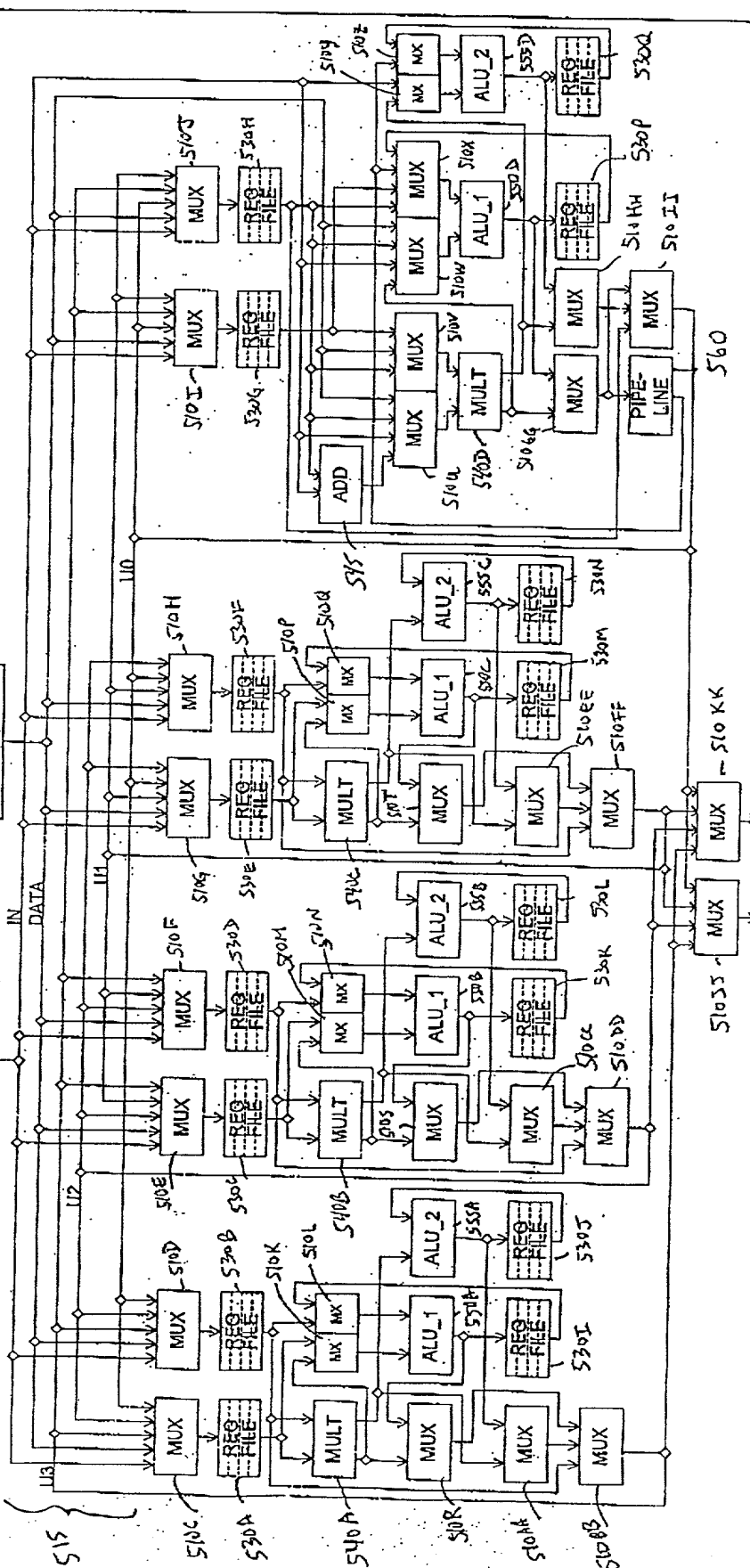
MUX

520

WRT
INPUT
MEMORY
READ

525

WRT
DATA
MEMORY
READ

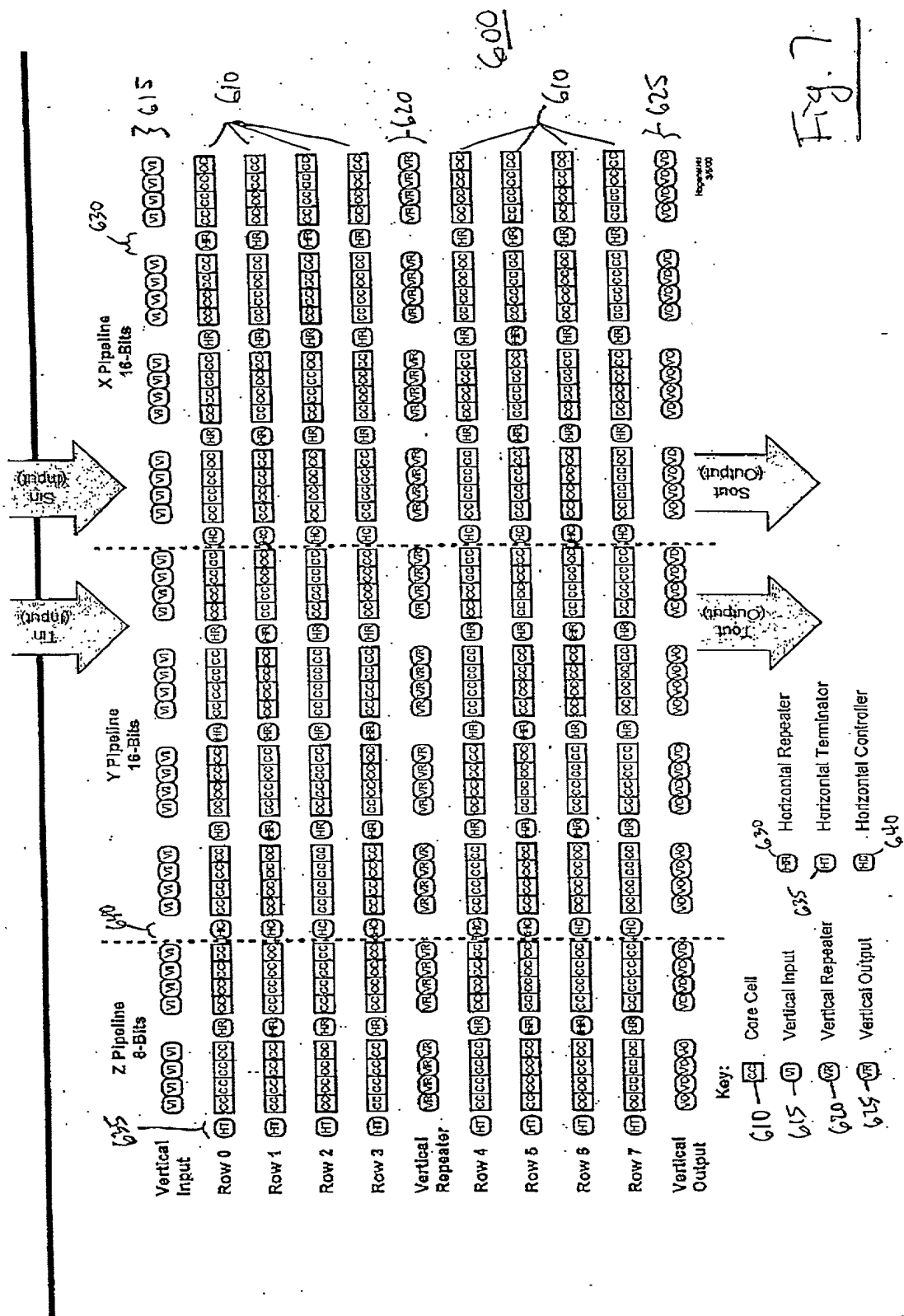


570

NODE OUTPUT
PIPELINE REGISTER &
BYPASS REGISTER

FIG. 6

500



1. The circuit is a 3-input, 2-output function generator.
 2. It consists of three 4-to-1 multiplexers (SA, SB, SC) and a 3-input, 2-output function generator block (650).
 3. The inputs to the multiplexers are: SA (Fn, Fw, Fsl, Ge), SB (Fn, F0, Ln, Le), and SC (Fw, Fsr, Ls, Lw).
 4. The outputs of the multiplexers are: A (input), B (input), and C (input).
 5. The function generator block (650) takes A, B, and C as inputs and produces two outputs: F (output) and G (output).
 6. The output F (output) is connected to a flip-flop (Flip Flop) and an SFF (Set-For-Force) block.
 7. The output G (output) is connected to a register (Register 32000).
 8. The circuit is labeled with various components and their connections, including a 655 timer and a 670 timer.

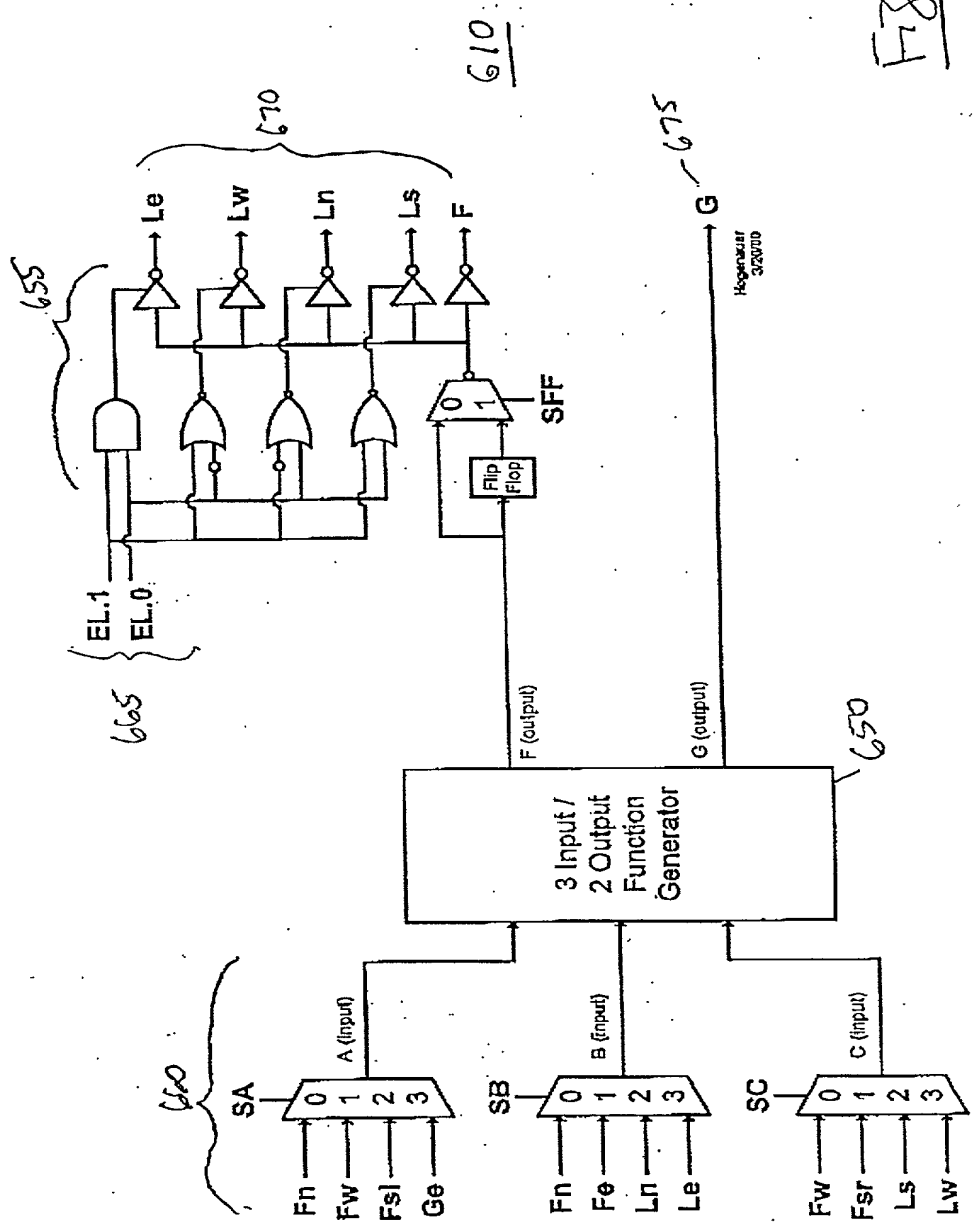


Fig. 8

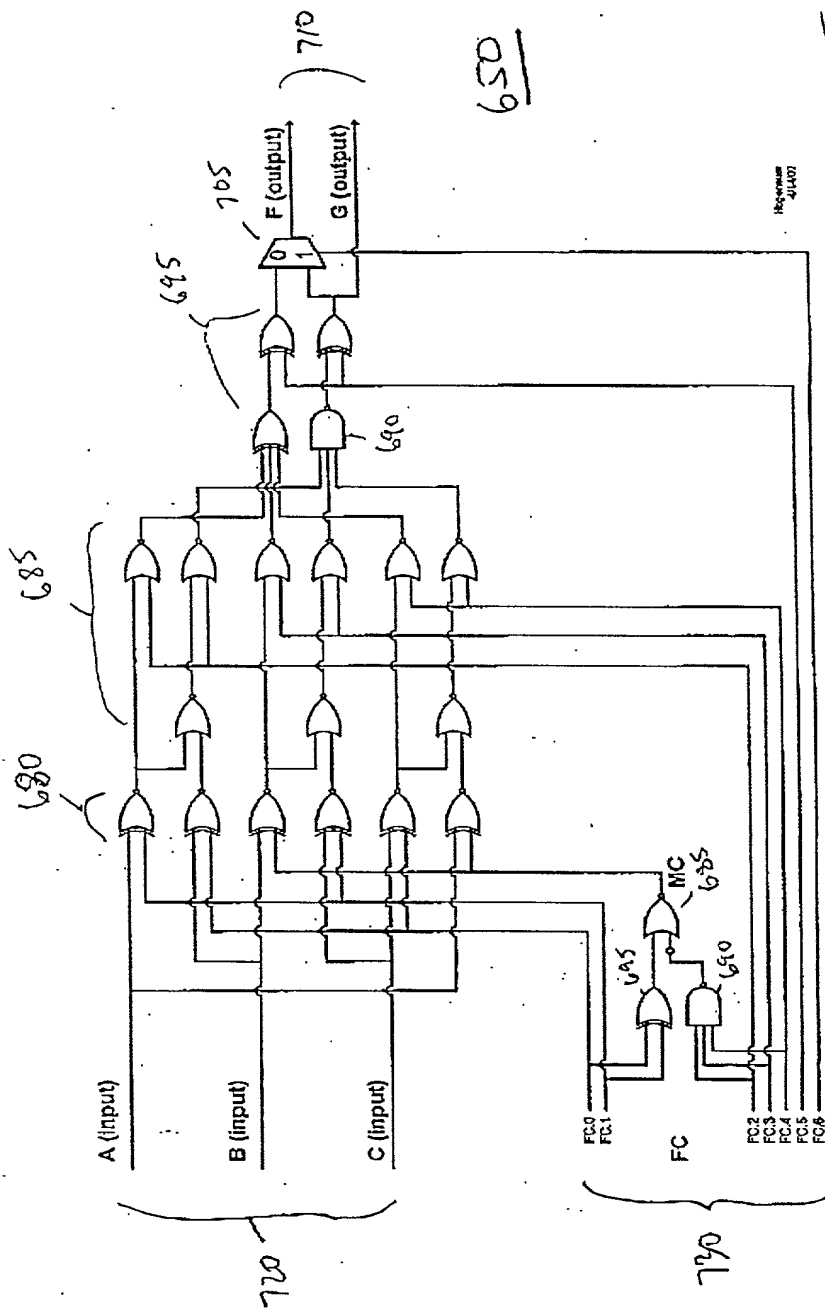
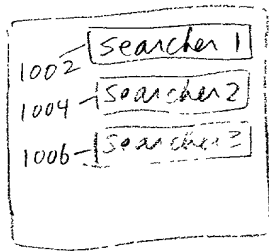
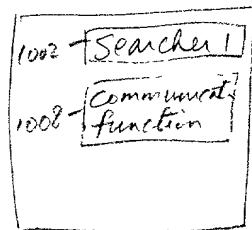


Fig. 9

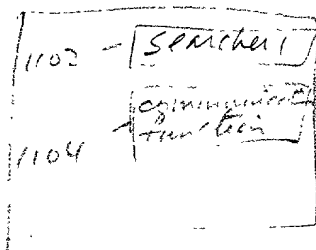


At power-up

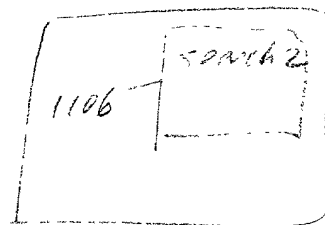


After system acquisition

FIG. 10

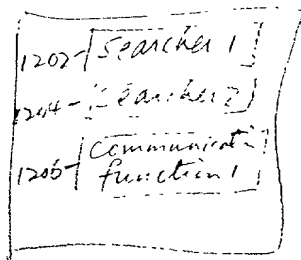


Before re-allocation

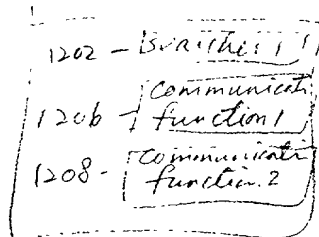


After re-allocation

FIG. 11

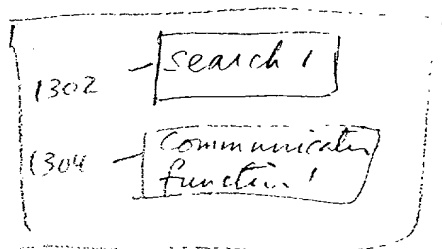


Before re-allocation

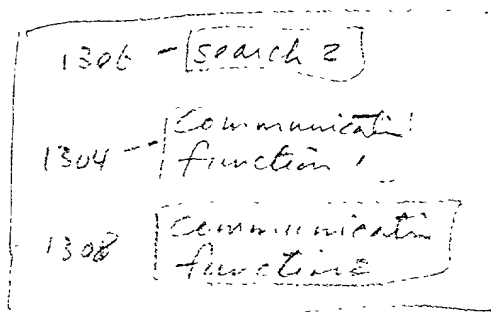


After re-allocation

FIG 12



Before re-allocation



After re-allocation

FIG. 13